

## ABSTRACT

5 A frame rate controller 20 is provided for controlling  
the frame refresh rate of an active matrix display. The  
controller 20 comprises a first circuit such as a  
preloadable synchronous counter 21 which counts vertical  
synchronisation signals VSYNC and supplies an enable  
signal FE for every Nth frame of data, where N is an integer  
10 greater than zero and is selectable. A gating arrangement  
26 is controlled by the enable signal FE so that an active  
matrix display is refreshed for every Nth frame of data,  
thus allowing a reduction in power consumption of the  
display.

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